Design of high precision time synchronization system based on GPS/ BD dual mode

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Abstract: In this paper, a new method of clock disciplining based on GPS/BD dual-mode receiver is proposed, which can improve the estimation accuracy of clock bias by fusing the GPS clock bias data and the BD clock bias data. In addition, the use of unbiased FIR filtering algorithm to filter the clock bias data to improve the accuracy of the clock filter. According to the experimental results, the time synchronization precision of the proposed method is 50ns, which is better than that based on single mode GPS and single mode BD time synchronization system.

Keywords: GPS/BD dual-mode, time synchronization, PLL; unbiased FIR filter

1. Introduce

In 2020 Global will enter largely the era of 5G technology, when people can enjoy thousands times speed of network, communication and so on each service. It requests clock system with high accuracy and stability, even clock precision reach the nanosecond level. Those system are required to meet the time synchronization strictly.

Satellite time service is the mainstream time synchronization technology, wherein the GPS (global navigation satellite system) is the most mature and become popular, with wide coverage and high precision [1].However, the GPS belongs to US government and has potential risk, such as deliberately reduced accuracy, even in war and other uncertain factors may lead to other areas cannot use the GPS service, causing a big threaten for GPS applications in china.

BD satellite navigation system (BD) is the construction of autonomous and independent operation of the satellite navigation system. It will provide global users with all-weather, all-day, high-precision positioning,

navigation and timing services after full completion. BD Can work independently for our country electric power, navigation, survey and other fields for service.

Traditional GPS/BD dual-mode technology is the GPS timing signal as a priority, BD timing signal as a backup, and then use BD timing signal when GPS signal does not work normally. The time synchronization scheme based on single mode receiver, its precision is generally low and performance of the system index has the potential to be improved.

In this paper, a new method of time synchronization based on GPS/BD dual-mode receiver is proposed, which can improve the estimation accuracy of clock bias by fusing the GPS clock bias data and the BD clock bias data. In addition, the use of unbiased FIR filtering algorithm to filter the clock bias data to improve the accuracy of the clock filter. According to the experimental results, the time synchronization precision of the proposed method is 50ns, which is higher than that based on single mode GPS and single mode BD time synchronization system.

2. System General Design

2.1 Principle of Time Synchronization

Satellite timing signal has the characteristics of long-term stability and high accuracy, utilizing Satellite time technology to generate a stable second pulse signal (1PPS) periodically to tame the local clock crystal, frequently local clock crystal output signal with high stability, so the system can obtain an time frequency signal which has good attributes of short-term accuracy and long-term stability[2][3]. In this paper, local clock crystal is OCXO(Oven Controlled Crystal Oscillator).

Control principle of the system is the mechanism of [4] PLL, using PID control algorithm to adjust the input signal of OCXO, the output signal and the input signal to maintain a stable relationship. The system consists of satellite receiving module, time interval measurement module, data processing module and OCXO, time interval measurement module programming implementation in FPGA, the data processing module is programmed by ARM. The principle diagram of time synchronization method is shown in figure 1.
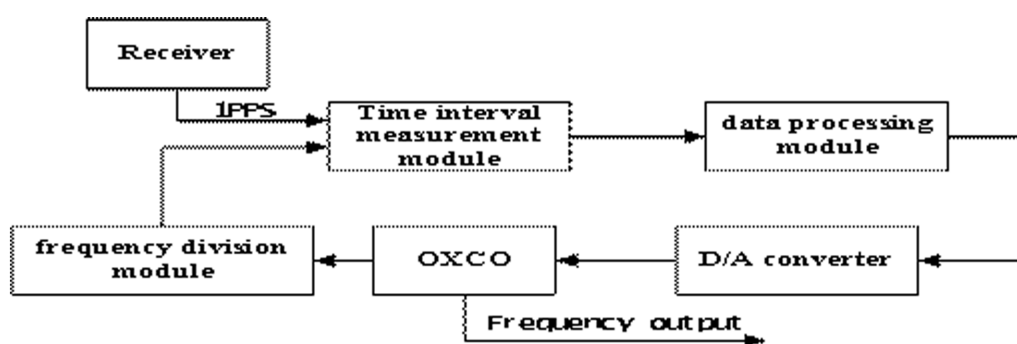

Fig. 1 The schematic diagram of frequency source taming system

An input time interval measurement module is 1PPS, and another input is periodical 1Hz signal from OCXO frequency division, Time interval measurement module includes the functions of pulse counting, frequency division and frequency measuring; The data processing module use unbiased FIR filter algorithm to process the clock data, improving the filtering precision. The PID control algorithm calculate frequency deviation that OCXO relative to the GPS, and D/A converter converts it to analog voltage as the OCXO input, output frequency adjust temperature crystals, adjusting the output frequency of OCXO.

2.2 Mechanism Of Dual-Mode Fusing

This paper presents a new time synchronization method based on GPS/BD dual-mode, by building the weight coefficient to fuse the GPS clock bias estimation data and the BD clock bias estimation data, realizing clock tame system based on GPS/BD dual-mode fusion. Unbiased FIR filtering algorithm is used to eliminate the error of GPS signal instability and measurement caused by the clock data, improve the filtering accuracy of clock bias, gain high precision clock bias estimation and clock bias speed estimation. The fusion formula is as follows:

$$x = \alpha \cdot x_{GPS} + \beta \cdot x_{BD} \tag{1}$$

$$\alpha = \frac{x_{BD}}{x_{GPS} + x_{BD}}, \beta = \frac{x_{GPS}}{x_{GPS} + x_{BD}} \tag{2}$$

In the formula, x is the clock difference estimation after fusion, α and β is the fusion coefficient of clock difference, x_{GPS} is based on GPS clock difference estimation and x_{BD} is based on BD clock difference estimate.

$$\dot{x} = \varepsilon \cdot \dot{x}_{GPS} + \varphi \cdot \dot{x}_{BD} \tag{3}$$

$$\varepsilon = \frac{\dot{x}_{BD}}{\dot{x}_{GPS} + \dot{x}_{BD}}, \varphi = \frac{\dot{x}_{GPS}}{\dot{x}_{GPS} + \dot{x}_{BD}} \tag{4}$$

In the formula, $\dot{x}$ is the clock rate estimation value after fusion, ε and φ is the fusion coefficient of clock rate estimation value, $\dot{x}_{GPS}$ is based on GPS clock rate estimation, $\dot{x}_{BD}$ is based on BD clock rate estimation.

GPS signal and BD signal all contain different noise components. The method proposed in this paper can reciprocal offset some noise and improve the accuracy of the proposed method.

3. Software Design And Algorithm

3.1 Software design

The software part consists of FPGA and ARM. In FPGA, time interval measurement module accurately calculate time interval between 1PPS and 1Hz signal rising edge. FPGA uses Verilog hardware description language and combined with its own IP core is relatively easy to achieve pulse counting, frequency division and frequency measurement and other functions. So this article does not consider the FPGA software programming.

The data processing module is programmed by ARM, perform data processing program to calculate, analyze and judge the time interval from time interval measurement module, and calculate the frequency deviation, D/A converter correct OCXO with inputting frequency deviation. The work process of the system can be abstracted into 4 states, including the Initialization state, track state, stable state and punctuality state, which mainly based on the state of the receiver receives the signal and filter the clock bias estimation value to distinguish. The system state transition diagram is shown in figure 2.
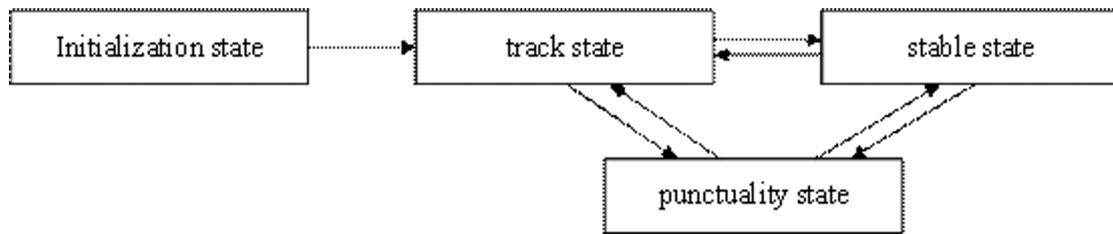
Fig. 2 The diagram of system state transition

3.2 Algorithm Design

Unbiased FIR algorithm: finite impulse response filter, also known as non recursive filter, is the most basic components of digital signal processing system, it can ensure any amplitude frequency characteristics and a strictly linear phase frequency characteristics, at the same time the unit sample response is limited, so the filter is stable system.

To some extent, achieving the precise control of OCXO key lies in using filter algorithm to improve filter accuracy of clock bias. It first proposed by a foreign Professor, Yuriy S. Shmaliy, application of unbiased FIR filter among receiver clock bias estimation, the formula derivation of the corresponding description in the literature, Through the experimental data analysis, he concluded that the FIR filter in the receiver clock bias estimation is better than the results of the kalman filter[5][6], as well as compared with the Kalman filter, its Allan variance is slightly better. In the implementation of the software, the unbiased FIR filtering algorithm is improved into an iterative form, which doesn't need to store a large amount of data, which is convenient for the portability of the algorithm.

The idea of unbiased FIR algorithm through collecting a certain number of observations using convolution formula to calculate the requirements of the state estimate, computation formula is as follows:

$$\omega(n) = \sum_{i=0}^{N_k-1} W(i)\lambda(n-i) \tag{5}$$

In the formula, $\lambda(n)$ is the clock bias observation, the N_K is the sampling period, and the $W(i)$ is the convolution coefficient.

$$W(i) = \begin{vmatrix} \xi_k(i) & 0 & ... & 0 \\ 0 & \xi_{k-1}(i) & ... & 0 \\ ... & ... & ... & ... \\ 0 & 0 & ... & \xi_0(i) \end{vmatrix} \tag{6}$$

The unbiased FIR filtering algorithm is applied to this system, the basic idea is used by low order state estimation to calculate high order measurements, and so on, finally, get the clock bias estimation and clock bias speed estimation. The calculation method of clock bias estimation is as follows:

$$\omega_1(n) = \sum_{i=0}^{N_1-1} \xi_1(i)\lambda_1(n-i) \tag{7}$$

The first order observation $\lambda_1(i)$ and the convolution coefficient $\xi_1(i)$ are calculated in the sampling period N_1, and the first order state estimation $\omega_1(n)$, namely the clock bias estimation value, is obtained.

The second order state observation $\lambda_2(i)$ is obtained by the first order state estimation $\omega_1(n)$, and the formula is as follows:

$$\lambda_2(i) = \frac{1}{\tau}(\omega_1(i) - \omega_1(i-1)) \tag{8}$$

After getting the N_0 second order observation $\lambda_2(i)$, the convolution calculation is performed with the convolution coefficient $\xi_0(i)$, and the second order state estimation $\omega_2(n)$, which is the clock bias speed, is obtained, and the formula is as follows:

$$\omega_2(n) = -\sum \xi_0(i)\lambda_2(n-i)$$

$$= -\sum \xi_0(\ )(\omega_1(i) \quad \omega_2(i-1)) \tag{9}$$

The system uses digital PID control algorithm to calculate the voltage control word, digital PID control algorithm which is based on the principle of PID control algorithm to apply in computer or hardware control system is a program algorithm, and it has the characteristics of stable, fast and accurate. In this design, we can simplify the programming and reduce the occupation of memory cells. The clock bias and the clock rate of the control algorithm are obtained by the unbiased FIR filter. The clock model in the system is as follows:

$$x(i+1) = x(i) + \dot{x}(i)$$
$$\dot{x}(i+1) = \dot{x}(i) + u(i) \tag{10}$$

In the equation, $x(i)$ is a clock bias, $\dot{x}(i)$ is clock rate, $u(i)$ is control word. Because the OCXO has good short-term stability, assume that clock speed of control cycles is constant, the clock speed is accumulated, the next control node clock difference is:

$$x(i+n) = \dot{x}(i) * n \tag{11}$$

n is the control cycle. After a period of n, the clock bias is eliminated to zero, so the control word $u(i)$ that is required to be applied can be expressed as follows:

$$u(i) = k_d \cdot (-\dot{x}(i)) + k_p \cdot \frac{-x(i)}{n} \tag{12}$$

In the above formula, k_d is the differential coefficient and k_p is the proportion coefficient, the clock bias adjustment schematic diagram is shown in figure 3:
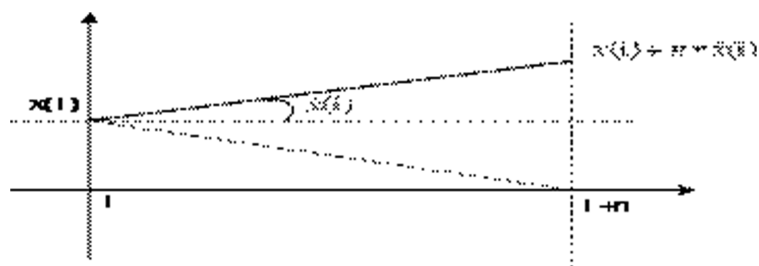

Fig. 3 The diagram of PID control calculation

The control word is converted to analog voltage by the D/A converter, and then input it to the OCXO to adjust output frequency of OCXO.

4. Experimental Result

In order to verify the new method of clock disciplining based on GPS/BD dual-mode receiver, respectively using single-mode BD timing signal, single-mode GPS and GPS/BD dual-mode timing signal fusion to discipline OCXO. We can calculate the clock bias between GPS second pulse signal and the 1PPS produced by the frequency division of the OCXO after taming. The sampling period is 150s, and 100 sets of data are acquired, and the unit of vertical coordinates is ns. The second pulse precision in three modes is shown in Fig. 4.

We can see from Figure 4, in the system of satellite navigation signal under normal operating conditions. After the system entering the locked state, phase tracking error which between GPS second pulse signal and the 1PPS produced by the frequency division of the OCXO remains within a certain range, In the time synchronization scheme based on single-mode receiver, the time synchronization accuracy based on single-mode GPS is better than that based on single-mode BD time synchronization system, however, its time synchronization accuracy is still greater than 60ns, and there is a big fluctuation; it improves the clock precision that GPS/BD dual-mode time synchronization method, time synchronization accuracy remains within 50ns. The new method of clock taming based on GPS / BD dual-mode receiver is better than the single-mode GPS or single-mode BD timing scheme.
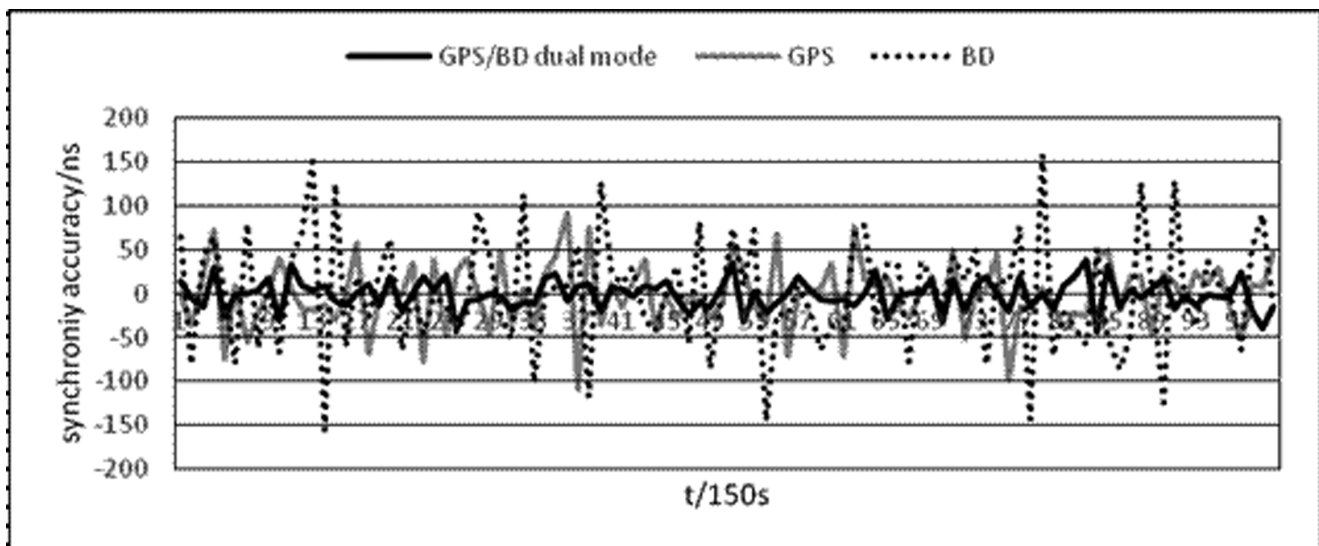

Fig. 4 second pulse precision

5. Conclusion

In view of the high needs of time synchronization accuracy in electric power, control communication and other fields, this paper puts forward a new method for clock disciplining based on GPS/BD dual-mode receiver, and has designed and implemented a clock tame system, which consists of ARM and FPGA. In addition, the design principle, software design flow and algorithm design of the dual mode fusion has described detailedly. Seen from the experimental results, clock precision has been improved by data fusion method, and time synchronization accuracy is more accurate, better than that based on single mode GPS and single mode BD time synchronization system, which could provide a higher accuracy and more accurate time frequency signal for each field.

Reference

[1] SHAN Qingxiao, YANG Jun. Review of satellite Disciplined Colck System[J], Journal of Test and Measurement Technology, 2009,23（5）:397-400.

[2] M. R. Mosavi. Use of Accurate GPS Timing based on Radial Basis Probabilistic Neural Network in Electric Systems[C]. International Conference on Electrical and Control Engineering，2010：2572-2575.

[3] Xie Qiang, Qian Guangdi. Design and realization of high precise frequency source based on timing GPS[J], Industrial Control Computer, 2007, 20（3）: 15-16.

[4] Beomsup Kim. Dual-loop DPLL gear-shifting algorithm for fast synchronization [J] . IEEE Transactions on Circuits and Systems-II : Analog and Digital Signal Processing, 1997, 44(7): 577.

[5] Shmaliy Y S. An unbiased FIR filter for TIE model of a local clock in applications to GPS-based timekeeping[J]. ieee transactions on ultrasonics, ferroelectrics, and frequency control, 2006, 53(5): 862-870.

[6] Shmaliy.S Y, Munoz-Diaz J, Arceo-Miquel L, et al. Optimum time step and memory for GPS-based unbiased FIR estimates of the local clock TIE model[C]. IEEE International Frequency Control Symposium Jointly with the 21st European Frequency and Time Forum, 2007, 291-296.