

A Fast Optical Spectrum Data Acquisition Method Based on FPGA and DSP

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Abstract. This paper presents a fast CCD optical spectrum data acquisition method based on FPGA, FIFO and DSP. Introduces a linear CCD timing sequence control signal generation and high speed ADC interface with FIFO and DSP in detail, publishes this design key parts FPGA logic schematic and VHDL source code, provides a general solution for universal high speed CCD optical spectrum data acquisition and analysis system.

Keywords: Linear CCD, FPGA, FIFO, DSP

1. Introduction

Fiber spectrometer is the key parts in portable Raman spectrometers, It is composed of Linear CCD detector , optical parts (filter, diffraction grating, lens etc) and data acquisition, store and processing circuit part, but how do to fast sample and save this optical spectrum data into PC is a critical issue for the fiber spectrometers. So this paper presents a powerful method of fast CCD data acquisition, introduces the method and key parts implement hardware schematic and FPGA VHDL source code in detail.

2. System design based on FPGA and DSP

Whole system level hardware design digram is showed as figure 1, In this design, ILX511 Linear CCD is selected as optical spectrum detector, in order to obtain high SNR and high resolution in this system, a high performance 18 bit SAR ADC chip AD7641 is used, also an asynchronous FIFO RAM has been used as bridge between the ADC and DSP, FPGA is used to generate variety CCD timing clock and asynchronous FIFO control signal. TMS320VC5509A DSP is used as a whole system center control unit, because of it's fast data processing ability, low power consumption and built in USB 2.0 port. so by using this DSP chip, the CCD sampling optical spectrum data can be fast transmitted to DSP internal SRAM and then do Raman data analyzing algorithm, also taking advantage of this DSP USB 2.0 port, the sampling data can be fast sent to PC. With DSP powerful McBSP communication port, the DSP chip can easy send the command to FPGA and laser control driver. TFT color display is a option in future product update.

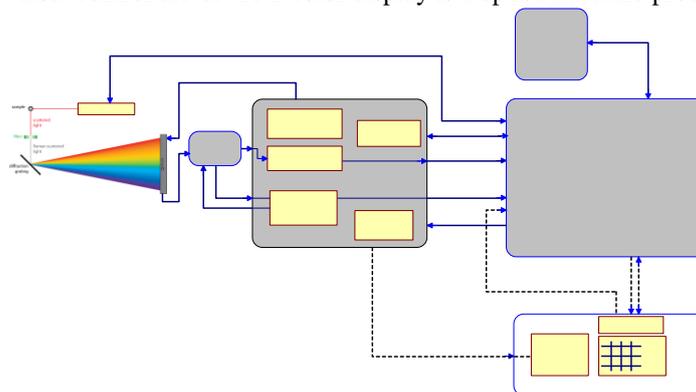


Fig 1. Raman Spectrometer System Diagram

3. Linear CCD Time Sequence Signal Generation and Optical Spectrum Data Acquisition

A. ILX511 linear CCD time sequence signal generation

The ILX511 is CCD linear image sensor, it's feature: 2048 pixels, 14 μm x 200 μm (14 μm pitch), Single 5 V power supply, ultra-high sensitivity, built-in sample-and-hold circuit, maximum clock frequency is 2MHz, its wavelength range from 400~ 1000nm, it is well fit to Raman Spectrum data analyzing wavelength range, when use a 785 nm laser source.

Figure 2 shows this CCD detector time sequence diagram, figure 3 shows its analog output waveform, so in order to driver ILX 511 CCD , external driver circuit has to provide two time sequence control signal : one is CCD clock signal ΦCLK , it's maximum frequency is 2Mhz, tpical working in 1Mhz. another is timing driver signal ΦROG . The ΦROG pulse period decides the scan a frame pixel time and CCD exposure time, since a frame has 2048 pixel + 38 dummy signal = 2086 clock pulse, so scanning a frame CCD pixel needs at least 2086 clocks signal period, and the true effective clock generated analog signal , which is sensitive optical exposure source, has only 2048 pulse. so CCD time sequence

signal generation module has to have function as follows: 1) generates Φ_{ROG} pulse, Φ_{ROG} period $> 20486 \times \Phi_{CLK}$ period; 2) generates more than 2086 clock pulse Φ_{CLK} ; 3) generates 2048 clock pulse with duty cycle 50% Φ_{ADC_CONST} , which is composed CCD output analog signal and synchronized to start ADC converter. The Φ_{CCD_ROG} negative pulse enable the CCD output effective and let the CCD exposed pixel convert analog signal output by CCD clk clock driving. So how to create these three control pulse is the design key point.

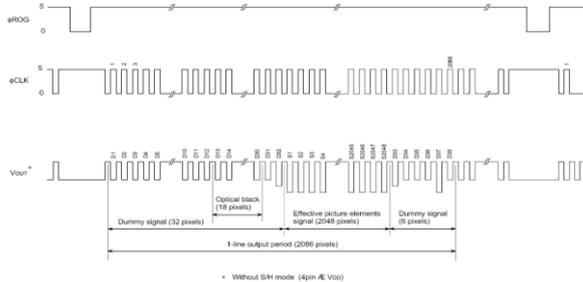


Fig 2 ILX511 Linear CCD Clock Timing Diagram

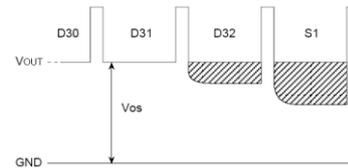


Fig 3 CCD Analog output

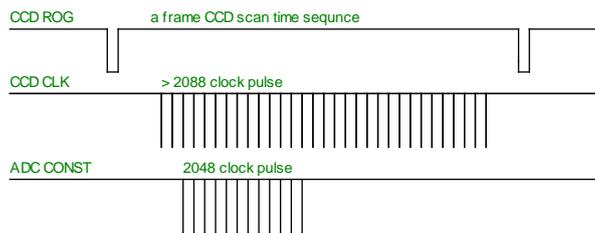


Fig. 4 3 key CCD control pulse waveform

Figure 4 displays this three control pulse waveform, and figure 5 presents their FPGA logic function schematic. In this design, a stable 20Mhz clock source can be obtained through FPGA internal PLL, Divide this 20 Mhz clock source into 1 MHz with 50% duty cycle using a divider, this 1Mhz clock function as whole CCD driving clock source, the CCD and ADC time sequence control signal generation module is shown in Figure 5. In order to obtain a Φ_{ROG} signal, use a 4 divider to get a 8 us width pulse as a ROG generator, the Φ_{ROG} period is controlled by receiving parameter through McBSP port coming from DSP.

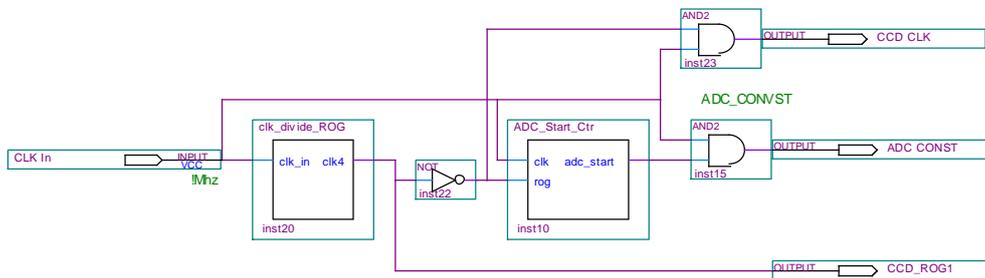


Fig 5 CCD and ADC time sequence control signal generation module diagram

In Figure 5, module inst20 implement the Φ_{ROG} pulse generation function, module inst10 implement the CCD clk and ADC start pulse signal. The figure 6 shows this signal generation simulation waveforms. Inst20 and inst10 mode VHDL code is present in follows. the inst10 VHDL is the same with inst17 in figure 7, difference is inst17 VHDL adds FIFO control function. As figure 6 show the simulation result, the function is exactly well meet the CCD control time sequence requirement.

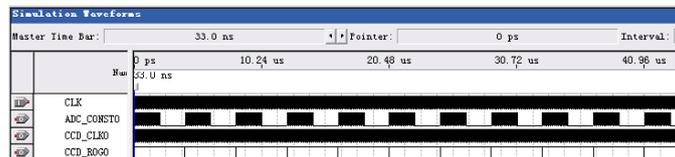


Fig6 CCD and ADC timing sequence generation waveform

B. CCD data sampling and transmit into DSP Internal SRAM

How do the CCD sampling data fast transmit to DSP internal SRAM is secondly key design point. Since TMS320VC5509A DSP has more rapidly operation speed when core clock frequency works in 200Mhz, and the ccd scan clock frequency is 1Mhz, if using the 1 Mhz pulse to directly trigger the DSP external interrupt source, the high data rate cannot be achieved to read data from the converter. Because Interrupt latencies prevent the DSP from reacting fast enough and even use a direct memory access (DMA) transmit data. since the high data tied up most of I/O port bandwidth, the Whole DSP working efficiency will drop too much, so an ideal solution is use FIFO as buffer bridge, when whole 2048 pixel of CCD signal has been sampled and saved to FIFO, the block data can be read in burst from FIFO to DSP SRAM through DMA mode.

Figure 6 give a whole CCD and FIFO control signal FPGA schematic, Lpm_counter1 is used only for simulation

ADC input data. Although Altera FPGA provides rich FIFO source, factual using has a lot of trick. The W_REQ and R_REQ has to set strictly , usually output signal W_full and R empty signal are used as a monitor judgment, but facul using R_REQ as external data start to read is more better than using W_full. from Figure 7, rdempty output signal provides a read FIFO effective signal, so use R_REQ as DSP external interrupt trigger signal, in DSP interrupt response routine, read whole 2048 data block, when DSP implement read EMIF, it generates a ARE signal, which can be utilized as synchronized FIFO read data clock signal R_clk; from the Fig6 schematic, ADC_StartCtr mode provides ADC start signal, and ADC busy output signal is used as FIFO write data clock signal , that means ,only when ADC finish one conversion, the ADC conveter data is valid and the sampling data can be saved to FIFO RAM, from Fig.9 , Fig.10, when R_Req is ready, ADC_out data is not effective, need wait for 6 r_clk clock, so using R_Req as DSP interrupt source, in DSP interrupt service routine, discard first 6 data and keep reading 2048 data using DMA counter. So from D[0] to D[2047] total 2048 sampling data can be read to DSP SRAM.

Fig. 8 shows the function implement simulation result of figure 6, from this waveform, the W_clk set in 10ns and r_clk is set 1ns, that means let r_clk is 10 times fast than W_clk , and result show read data bolck is fast 10 times than write data block. It successfullly solves the difficulty of ADC and DSP asynchronized data read and write speed.

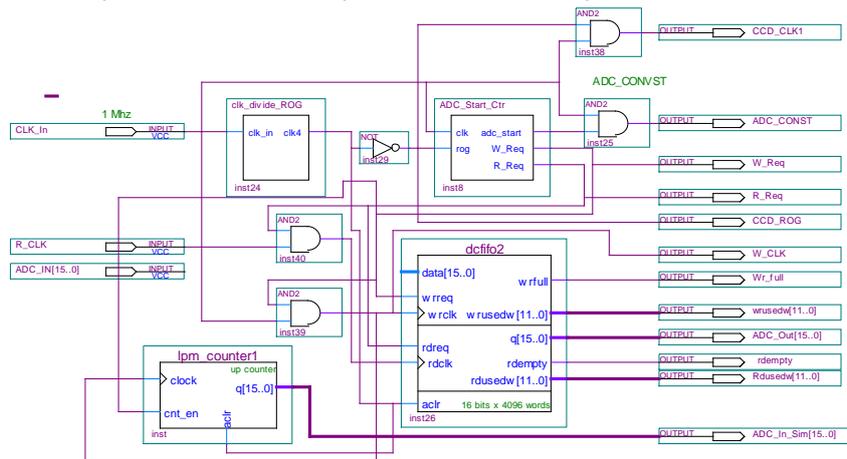


Fig. 7 CCD and FIFO control signal schematic

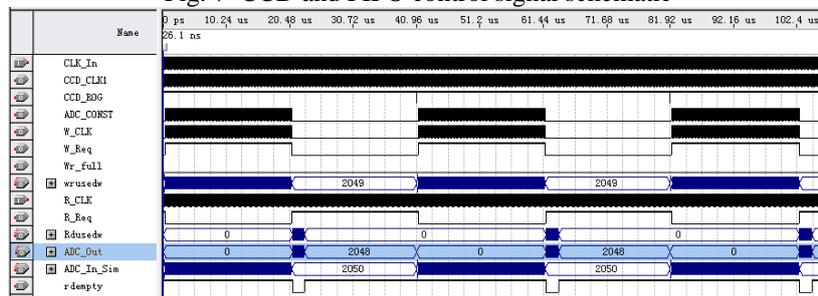


Fig.8 CCD and FIFO control signal simulation waveform

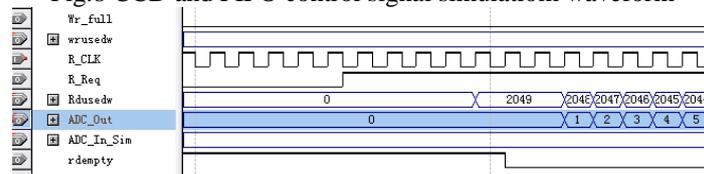


Fig.9 Data read initial side

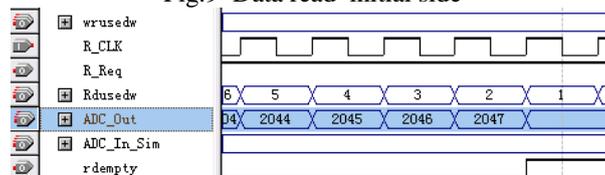


Fig.10. Data read end side

C. FPGA control mode VHDL Source Code

----- CCD ROG signal generation VHDL

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
entity clk_divide_ROG is
Port(clk_in: in std_logic;
      clk4: out std_logic);

```

```

end entity clk_divide_ROG;
Architecture behave of clk_divide_ROG is
signal clk10c: std_logic;
Signal div10cnt: unsigned( 15 downto 0);
begin
Process(clk_in)
begin
    if(clk_in'event and clk_in='1') then
        div10cnt<=div10cnt+1;
    end if;
    if(div10cnt<="0000000000000000") then
        clk10c<='1';
    elsif(div10cnt>"0000000000000001" and div10cnt<" 0001000001010100 ") then -- more than 2088
        clk10c<='0';
    elsif(div10cnt >= " 0001000001010101 ") then
        div10cnt<="0000000000000000";
    end if;
    clk4 <= clk10c ;
end process;
end architecture behave;

```

4. CCD, ADC , FPGA and DSP hardware Interface

Figure 11 shows the CCD, ADC, FPGA and DSP important wires connection associated with system sampling data transmit. The ADC7641 ADC chip is selected, it's an 18bit high performance SAR ADC with SNR 93 db, 2 MSPS, and its power supply only has 2.5 V and differential input range is $\pm 2.5V$, also it's power consumption has only 75mw, this extraordinary features is especially well suitable for portable and handheld Raman optical analysis instrument. In this design set ADC mode in 16 bit parallel, and sampling mode set in normal 1.5 MSPS.

TMS320VC5509A has external memory interface(EMIF) with SARM and SDRAM, and six DMA controllers, it's external memory space is divided into 4 spaces by CE0~CE3, in this design, CE2 is used to select memory space from address 0x80,0000 to 0xc0,0000; so use 0x80,0000 to 0x0x80,0800 total 2048 byte external memory space as FIFO source address, and assign internal SRAM 0x 02,0000 to 0x020800 as DMA destination memory space.

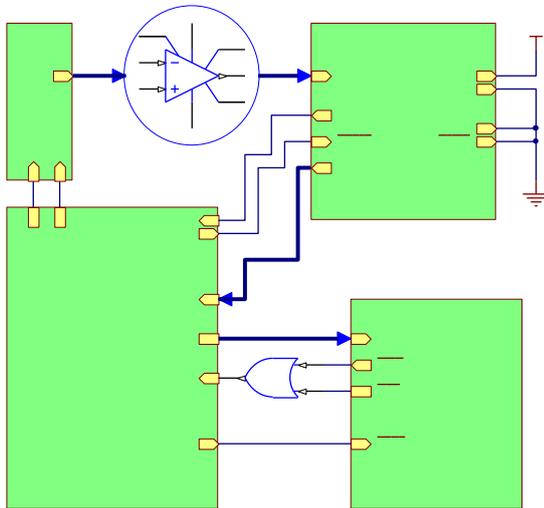


Fig. 11 CCD, ADC , FPGA and DSP Interface

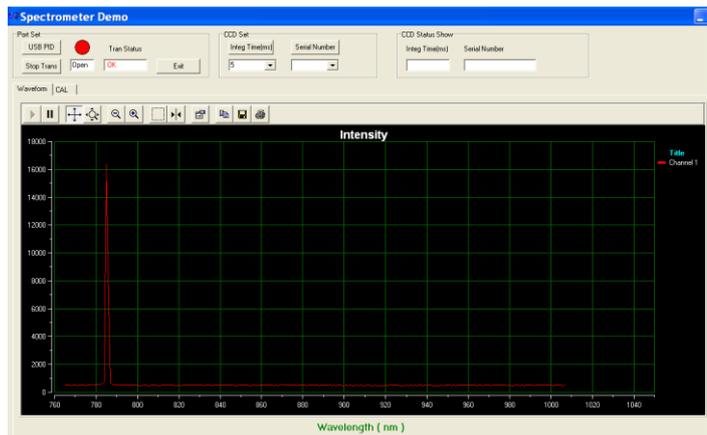


Fig 12 Optical spectrum sampling display

Figure 12 shows a 785nm laser source optical spectrum waveform, this waveform indicates that the whole system data sampling is success and the optical spectrum data can be fast transmitted to Pocket PC though USB 2.0.

5. Conclusions

Since FPGA is based on SRAM filed programmable array, so it can be composed of different size and depth of FIFO RAM. by using FPGA, variety CCD timing sequence control signal can be flexibly created, for different clock frequency CCD, just change the correspond conversion speed ADC chip, change FIFO reading and writing clock frequency, the ADC sampling data can be fast transmitted to DSP internal SRAM, meanwhile, DSP can implement real time algorithm and then transmits data to PC through it's USB port. Therefore this design provides a comprehensive optical spectrum data acquisition method.

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